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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/599,250	06/22/2000	Fabio M. Chiussi	Chiussi 19-7	7832

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EXAMINER	
ABELSON, RONALD B	

ART UNIT	PAPER NUMBER
2666	3

DATE MAILED: 08/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/599,250	CHIUSSI ET AL.	
	Examiner	Art Unit	
	Ronald Abelson	2666	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 June 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 June 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Specification

1. The disclosure is objected to because of the following informalities: Page 1 line 6 lists an attorney docket number.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 1 recites the limitation "said transmitted data packets" in line 11. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-6, 9, 10, 12-17, 19-22, and 26-30 rejected under 35 U.S.C. 102(e) as being anticipated by Shinohara (US 6,067,298).

Regarding claims 1, 16, 21, Shinohara teaches a method for transferring data through a packet switch (fig. 1 box 102) while providing differentiates Quality-of-Service QoS (fig. 1: CBR,VBR,ABR,UBR) guarantees to respective traffic flows.

Shinohara teaches storing received data packets associated with said traffic flows in a plurality input buffer (fig. 1 box 20, col. 6 lines 6-11). Regarding a plurality of input buffers, see fig. 8 boxes 20.

Shinohara teaches grouping said traffic flows by QoS classes, each of said QoS classes having a priority level (fig. 1 box 24 25, CBR, VBR, ABR, UBR, col. 6 line 65 - col. 7 line 2). Note, from highest to lowest the prioritization is CBR, VBR, ABR, and UBR.

Shinohara teaches selecting data packets for transmission to a switch fabric (fig. 1 box 102) according to a first plurality of schedulers (fig. 1 boxes 22, col. 7 lines 6-9). Note, the ATM cell is sent from internal queue (fig. 1 box 23 to the switch fabric (fig. 1 box 102).

boxes 109, col. 7 lines 12-15). Note, by controlling the competition between cell transfer requests, the examiner maintains that the interclass priority control section (fig. 1 box 109) is assigning bandwidth to the selected data packets. Regarding a second plurality of schedulers, a plurality of interclass priority control sections is shown in fig. 8.

Shinohara teaches storing said transmitted data packets in a plurality of output buffers in said switch fabric (fig. 1 box 30, col. 6 lines 10-11). Regarding a plurality of output buffers in said switch fabric, see fig. 8 boxes 30.

Shinohara teaches adapting the operation of at least one of said first and second schedulers in response to a determination that a utilization level of any output buffer has exceeded a threshold parameter (fig. 1 boxes 30, 102, 20, col. 8 lines 6-20, input buffer module section 20 ceases to transmit cells).

Regarding claim 16, in addition to the limitations previously listed, transmitting data packets to a respective plurality of output buffers (fig. 1, 8 box 30) according to QoS class priority levels (fig. 1 box 32, col. 7 lines 25-28).

Regarding claim 16 and 21, in addition to the limitations previously listed, halting transmissions to any of said

plurality of output buffers utilized beyond said threshold parameter (col. 8 lines 19-21).

Regarding claim 21, in addition to the limitations previously listed, a third plurality of schedulers for selecting data packets for transmission to respective output ports (fig. 1 box 113, col. 7 lines 28-33). Regarding a third plurality of schedulers, see fig. 8 boxes 113. Note, the output port is located within the interclass priority control section (fig. 1 box 109).

Regarding claim 21, in addition to the limitations previously listed, a plurality of output buffers (fig. 8 boxes 30), coupled to said third plurality of schedulers (fig. 1 box 113, col. 7 lines 28-33), for holding data packets before transmission to output ports.

Regarding claim 2 choosing the data packets to be transmitted out of said plurality of output buffers according to a third plurality of schedulers (fig. 1 box 113, col. 7 lines 28-33). Regarding a third plurality of schedulers, see fig. 8 boxes 113.

Regarding claim 3, grouping comprises the step of grouping said traffic flows according to traffic flow destination and QoS requirements (destination output line and service class type, col. 6 line 65 - col. 7 line 2).

Regarding claim 4, the method of claim 3, wherein said destination comprises an output of an egress port card (fig. 1 see egress port cards labeled CBR, VBR, ABR, and UBR) coupled to said switch fabric (fig. 1 box 102).

Regarding claim 5, each scheduler in said first plurality of schedulers (fig. 1 boxes 22) is a class-specific per-flow scheduler. Note, each class has a unique flow scheduler (fig. 1 box 22).

Regarding claim 6, each scheduler in said second plurality of schedulers is a per-QoS class port scheduler (fig. 1 box 109, col. 7 lines 12-15). See fig. 1, data from different QoS classes are input into the scheduler (fig. 1 box 109).

Regarding claims 9, 17, 19, applying selective backpressure to respective ingress port cards to prevent further transmission of data packets to any of said respective plurality of output

buffers for which the threshold parameter has been exceeded (col. 8 lines 6-20), said plurality of output buffers for which the respective threshold parameter has been exceeded being congested (col. 8 lines 6-7). Regarding the output buffers being congested, the examiner corresponds the total buffer use exceeding a threshold value with the buffers being congested.

Shinohara teaches determining whether said respective threshold level of each of said congested plurality of output buffers continues to be exceeded (fig. 11 box 301, col. 10 line 56 - col. 11 line 4) and resuming transmission to any congested respective plurality of output buffers when each respective said threshold parameter is not exceeded (fig. 11 box 301, col. 10 line 56 - col. 11 line 4).

Regarding claims 10, 20, and 22, each scheduler of said first plurality of schedulers (fig. 1 box 22) resides in ingress port cards (fig. 1 box 20).

Shinohara teaches each scheduler of said second plurality of schedulers (fig. 1 box 109) resides in said ingress port cards (fig. 1 box 20).

Shinohara teaches Shinohara teaches each scheduler of said third plurality of schedulers (fig. 1 box 113) resides in said switch fabric (fig. 1 box 102, 30). Note, the examiner maintains

that the core switch (fig. 1 box 102) and output buffer of the core switch (fig. 1 box 30) can be viewed as one unit.

Shinohara teaches said plurality of input buffers (fig. 1 box 20) reside in said ingress port cards. Note, the input buffer (fig. 1 box 20) is an ingress port card.

Shinohara teaches said plurality of output buffers (fig. 1 box 30) reside in said switch fabric (fig. 1 box 30, 102). Note, the examiner maintains that the core switch (fig. 1 box 102) and output buffer of the core switch (fig. 1 box 30) can be viewed as one unit.

Regarding claim 22, in addition to the limitations previously listed, said output ports (fig. 1 box 113) reside in said switch fabric (fig. 1 box 102, 30).

Shinohara teaches said ingress port cards (fig. 1 box 20) are coupled to the switch fabric (fig. 1 box 102).

Regarding claim 12, the switch fabric (fig. 8 box 102) comprises at least one module having a respective plurality of output buffers (fig. 8 boxes 30).

Regarding claim 13, each of the first plurality of schedulers (fig. 1 box 22) is associated with a respective QoS class (fig. 1 CBR, VBR, ABR, UBR).

Regarding claim 14, each of the plurality of output buffers (fig. 1 box 30) supports aggregated traffic flows of a defined QoS class. Note, fig. 1 box 30 supports traffic classes CBR, VBR, ABR, and UBR.

Regarding claim 15, each of said third plurality of schedulers (fig. 1 box 113) is associated with a respective output of said switch fabric (fig. 1 box 30 see CBR, VBR, ABR, and UBR).

Regarding claim 26, the switch fabric comprises a single module (fig. 1 box 30) with a plurality of output buffers (fig. 1 queues 31).

Regarding claim 27, the switch fabric comprises a multiple modules (fig. 8 boxes 30) with a plurality of output buffers (fig. 8 queues 31).

Regarding claim 28, each of said first plurality of schedulers (fig. 1 box 22) is associated with a respective QoS class of said configured flows. Note, one scheduler (fig. 1 box 22) is associated with each QoS class.

Regarding claim 29, the plurality of output buffers (fig. 1 boxes 31 are coupled to traffic aggregates called QoS channels (fig. 8 box 30, CBR, VBR, ABR, UBR).

Regarding claim 30, each one of said third plurality of schedulers (fig. 1 box 113) is associated with a respective output of the switch fabric (fig. 1 see output 50).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to

point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 7, 18, 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shinohara as applied to claim 1, 16, and 21 above, and further in view of Regache (US 5,579,312).

Although Shinohara teaches a second plurality of schedulers (fig. 1 box 109) for selecting groups of configured traffic flows for transmission of data (fig. 1: CBR, VBR, ABR, UBR), the reference is silent on each of the schedulers being a Guaranteed Bandwidth Scheduler.

Regache teaches a Guaranteed Bandwidth Scheduler based upon minimum bandwidth guarantees (fig. 1, guarantee transmission of cells at a particular rate, col. 5 lines 53-57).

Therefore it would have been obvious to one of ordinary skill in the art, having both Shinohara and Regache before him/her and with the teachings [a] as shown by Shinohara, a method for transferring data through a packet switch while providing differentiates Quality-of-Service QoS guarantees to respective traffic flows, and [b] as shown by Regache, a

Guaranteed Bandwidth Scheduler based upon minimum bandwidth guarantees, to be motivated to modify the system of Shinohara to incorporate within the second schedulers the Guaranteed Bandwidth Scheduler algorithm of Regache. This modification can be performed in software. This would improve the system of Shinohara by ensuring an equitable distribution of bandwidth to each of the QoS classes.

9. Claims 8 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shinohara as applied to claims 1 and 21 above, and further in view of Regache (US 5,579,312).

Although Shinohara teaches a third plurality of schedulers (fig. 1 box 113) for selecting groups of configured traffic flows for transmission of data (fig. 1: CBR, VBR, ABR, UBR), the reference is silent on each of the schedulers being a Guaranteed Bandwidth Scheduler.

Regache teaches a Guaranteed Bandwidth Scheduler based upon minimum bandwidth guarantees (fig. 1, guarantee transmission of cells at a particular rate, col. 5 lines 53-57).

Therefore it would have been obvious to one of ordinary skill in the art, having both Shinohara and Regache before him/her and with the teachings [a] as shown by Shinohara, a method for transferring data through a packet switch while

providing differentiates Quality-of-Service QoS guarantees to respective traffic flows, and [b] as shown by Regache, a Guaranteed Bandwidth Scheduler based upon minimum bandwidth guarantees, to be motivated to modify the system of Shinohara to incorporate within the third schedulers the Guaranteed Bandwidth Scheduler algorithm of Regache. This modification can be performed in software. This would improve the system of Shinohara by ensuring an equitable distribution of bandwidth to each of the QoS classes.

10. Claims 11 and 25 rejected under 35 U.S.C. 103(a) as being unpatentable over Shinohara as applied to claims 1 and 21 above, and further in view of Hiroki (JPO 06-284453). Note, the examiner has relied on the English translation of the document.

Shinohara is silent on the plurality of input buffers' capacity exceeds said respective plurality of output buffer's buffer capacity.

Hiroki teaches the plurality of input buffers' capacity (fig. 1 boxes 11_{1-n} and 14) exceeds said respective plurality of output buffer's buffer capacity (fig. 1 boxes 13_{1-n}). See paragraphs [0016] and [0017] in the English translation provided.

Therefore it would have been obvious to one of ordinary skill in the art, having both Shinohara and Hiroki before him/her and with the teachings [a] as shown by Shinohara, a method for transferring data through a packet switch while providing differentiates Quality-of-Service QoS, and [b] as shown by Hiroki, the plurality of input buffers' capacity exceeds said respective plurality of output buffer's buffer capacity, to be motivated to modify the system of Shinohara by adding a common buffer to the plurality of input buffers in Shinohara. This would improve the system by helping to prevent cell loss when the plurality of output buffers are full.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ronald Abelson whose telephone number is (703) 306-5622. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema Rao can be reached on (703) 308-5463. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ronald Abelson
Examiner
Art Unit 2666

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8/22/04

Seema S. Rao
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